IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF ILLINOIS
EASTERN DIVISION

HFT SOLUTIONS, LLC, Plaintiff, v. CITADEL SECURITIES LLC, Defendant.	Case No. 1:24-cv-13213 JURY TRIAL DEMANDED

DEFENDANT CITADEL SECURITIES LLC'S MOTION TO DISMISS

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The Supreme Court has long recognized that patent protection is not absolute and must be limited to promote innovation and scientific advancement. For example, while Section 101 of the Patent Act permits inventors to seek patent protection for "new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof," 35 U.S.C. § 101, there is an "important implicit exception: Laws of nature, natural phenomena, and abstract ideas are *not patentable*" because they are the "basic tools of scientific and technical work," *Alice Corp. Pty. Ltd. v. CLS Bank Int'l.*, 573 U.S. 208, 216 (2014) (emphasis added). Permitting opportunistic patent seekers to monopolize those ideas would "impede innovation more than it would tend to promote it." *Id.*

The three patents asserted by Plaintiff in this case are about "abstract ideas" and are thus "not patentable." *See id.* at 216. The claims of the Asserted Patents cover receiving, transmitting, generating, and converting data and signals to synchronize "clocks." Fundamentally, the claims are about manipulating data, which numerous courts have recognized is abstract. *See, e.g.*, *iLife Techs., Inc. v. Nintendo of Am., Inc.*, 839 F. App'x 534, 536 (Fed. Cir. 2021) ("We have routinely held that claims directed to gathering and processing data are directed to an abstract idea."); *Glasswall Solutions Ltd. v. Clearswift Ltd.*, 754 F. App'x 996, 998 (Fed. Cir. 2018) ("The claims merely require the conventional manipulation of information by a computer. We have often held similar conventional data manipulation to be abstract."). And there is nothing about the claims that would transform them into any more than the abstract idea at their core. The claims use well-known computer components that have been in existence for decades in the conventional ways they were designed to be used. *See Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1349 (Fed. Cir. 2019) (nothing transformative where claims "could be performed with off-the-shelf technology").

The Asserted Patents attempt to hide their abstract nature through "lengthy and numerous" claims. *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1351 (Fed. Cir. 2016) ("systems and methods for performing real-time performance monitoring of an electric power grid" not patent eligible, despite length). But all those extra words only use more space on the page to describe the same fundamentally abstract concepts, which amount to little more than sending information through well-known components. These claims are abstract and not eligible for patent protection. The Court should dismiss the complaint.

BACKGROUND

The Asserted Patents involve field-programmable gate arrays, or FPGAs, for high-frequency trading. High-frequency trading is a type of securities trading that relies on electronic tools to make extremely short-term investments. *See* Lemke and Lims, *Soft Dollars and Other Trading Activities* § 2:35 (West 2024-2025 ed.). Traders use computer algorithms to identify "temporary inefficiencies or pricing anomalies in the market," and then conduct "large trades at extraordinary speeds—sometimes in microseconds" to take advantage of the best available prices. *Id.* While many aspects of high-frequency trading are novel and unique, the fundamental building blocks for sending signals between computer systems are not.

High-frequency trading often uses FPGAs to carry out sophisticated, proprietary algorithms. FPGAs are a type of computer chip invented in the mid-1980s. As the Asserted Patents describe, FPGAs are not new. It was well-known at the time the Asserted Patents were filed that "[f]ield programmable gate arrays (FPGAs) may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-

grained parallelism." Ex. 1, '381 patent at 1:39-42.[1] Indeed, it was even known that "FPGAs are used in the financial industry in high frequency trading where the rapid processing of the FPGA is desired." *Id.* at 1:42-43.

The inventor of the Asserted Patents did not invent FPGAs. Nor do the Asserted Patents claim any trading algorithms that might use FPGAs to effectuate high-speed trading. Instead, the three Asserted Patents describe a "Field Programmable Gate Array with External Phase Locked Loop." The '305 patent claims an FPGA with a phase locked loop (PLL)—which essentially links the FPGA's data processing with an external clock—and '286 and '381 patents claim methods of processing data using such FPGAs.

The inventor of the Asserted Patents also did not invent phase locked loops. A phase locked loop is a method to ensure that data processed by an FPGA stays aligned with the timing of an external clock. Every clock has a "frequency," or unit by which it measures time. For example, a typical wall clock has a frequency of one second, because it ticks every second. The "phase" of the clock refers to where it is in its measurement cycle—for example, at the tick, halfway between ticks, three-quarters of the way to a new tick, and so on. Thus, a "phase locked loop" ensures the processes of the FPGA stay phase-aligned with the incoming clock's phase. *See All Computers, Inc. v. Intel Corp.*, No. 1:04-CV-00586-G, 2005 WL 4904818, at *10 (E.D. Va. Feb. 9, 2005) (reciting definition of phase locked loop from 1994 McGraw Hill Dictionary of Scientific and Technical Terms). These processes, including clock synchronization, were known long before the Asserted Patents. *See, e.g.*, Ex. 1, '381 patent at 2 (prior-art references include "Phase Frequency

[1] The asserted patents are part of the same patent family and share a specification. This brief cites the '381 patent unless otherwise stated.

Detector in PLL," "Phaselock Techniques," "Digital signal processing for an adaptive phase-locked loop controller," and "Time to Digital Converter used in All Digital PLL").

The claims of the Asserted Patents repackage these conventional components and known methods for synchronizing signals. For example, the '381 patent and '286 patent claim methods of processing data streams using an FPGA and phase locked loop to process market and order data. The '286 patent's method entails "receiving" certain data and signals at an "interface," or an intake point on the chip. From there, the method includes "transmitting," "generating," and "converting" steps that move the data and signals throughout the FPGA. The steps include "transmitting" signals to a "phase detector" to adjust clock differences. After the data and signals are transmitted to generic "computational circuitry," that computational circuitry performs unnamed operations on the data. Ultimately, the data is then transmitted by the FPGA. *See* Ex. 2, '286 patent at 28:14-29:15. The method specified by the '381 patent is similar. *See* Ex. 1, '381 patent at 28:22-25.

The system claims of the '305 patent repackage these conventional components and known methods for synchronizing signals, framing the claim as an FPGA and a phase control circuit capable of carrying out steps like those in the method claims. *See* Ex. 3, '305 patent at 28:9-29:49. The FPGA is made up of (1) an "interface," which brings data in from outside the FPGA; (2) a "deserializer," which converts data from a single stream into multiple data streams that can be transmitted in parallel to each other; (3) computational circuitry, which performs operations on the data; and (4) a "serializer," which turns the parallel data streams back into a single stream. *See id.* at 28:9-29:16. The phase control circuit, meanwhile, is separate from the FPGA, and ensures the data transmitted from the FPGA stays phase-aligned with the clock data brought into the FPGA. *See id.* at 29:16-48. None of these components are new.

ARGUMENT

I. THE CLAIMS OF THE ASSERTED PATENTS ARE NOT PATENT ELIGIBLE

"[A]bstract ideas are not patentable" under 35 U.S.C. § 101. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 573 U.S. 208, 216 (2014). Courts evaluate claims challenged under § 101 by applying a two-step framework set forth by the Supreme Court. *See id.* at 216-24. First, the court determines "whether the claims at issue are directed to a patent-ineligible concept," namely, laws of nature, natural phenomena, and abstract ideas. *Id.* at 217. Second, the court "consider[s] the elements of each claim both individually and as an ordered combination to determine whether the additional elements transform the nature of the claim into a patent-eligible application." *Id.* (internal quotation marks omitted). The Supreme Court has "described step two of this analysis as a search for an 'inventive concept—i.e., an element or combination of elements that is sufficient to ensure that the patent in practice amounts to significantly more than a patent upon the ineligible concept itself." *Id.* at 217-218 (cleaned up). "Those 'additional features' must be more than 'well-understood, routine, conventional activity.'" *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 715 (Fed. Cir. 2014).

Patentability under 35 U.S.C. § 101 is a threshold legal issue. *See Bilski v. Kappos*, 561 U.S. 593, 602 (2010). Patent eligibility is "a question of law, based on underlying facts" and evaluated according to Federal Circuit law. *SAP Am., Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1166 (Fed. Cir. 2018). The Federal Circuit has "repeatedly recognized that in many cases it is possible and proper to determine patent eligibility under 35 U.S.C. § 101 on a Rule 12(b)(6) motion." *Genetic Techs. Ltd. v. Merial L.L.C.*, 818 F.3d 1369, 1373 (Fed. Cir. 2016); *see also, e.g.*, *ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 773-75 (Fed. Cir. 2019) (affirming dismissal under Rule 12(b)(6)).

A. *Alice* Step 1: The Claims Are Directed to the Abstract Idea of Synchronizing Signals

Step 1 of the *Alice* framework asks whether the claims are "directed to" a patent-ineligible concept. The Federal Circuit has "described the first-stage inquiry as looking at the focus of the claims, 'their character as a whole'." *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350, 1353 (Fed. Cir. 2016).

The claims of the Asserted Patents are directed to an abstract idea—namely the idea of synchronizing data processing with a clock. *See* Ex. 1, '381 patent at claim 1 (steps include "receiving . . . a clock signal," "generating . . . a receiver side clock signal," "transmitting . . . the receiver side clock signal," "generating . . . a second clock signal," and "generating . . . a transmitter side clock signal"); Ex. 2, '286 patent at claim 1 (steps include "receiving . . . a first clock signal," "providing . . . a clock signal," "generating . . . a first receiver side clock signal," "transmitting . . . the first receiver side clock signal," "generating . . . a second clock signal," "generating . . . a first transmitter side clock signal," "transmitting . . . the first transmitter side clock signal"); Ex. 3, '305 patent at claim 1 (FPGA "configured to," for example, "receive," "transmit," "convert," "generate," and "perform . . . operations" on data and signals, phase control circuit "configured to," for example, "compare," "generate," "receive," and "transmit" data and signals).

Each claim at its core is about moving data through conventional computer processing components in synchronization with clock signals. It is well-established that mere manipulation of data is an abstract idea. *See, e.g.*, *Beteiro, LLC v. DraftKings Inc.*, 104 F.4th 1350, 1355-56 (Fed. Cir. 2024) (claims directed to "detecting information, generating and transmitting a notification based on the information, . . . , and processing information" are not patent eligible); *iLife Techs., Inc. v. Nintendo of Am., Inc.*, 839 F. App'x 534, 536 (Fed. Cir. 2021) ("We have routinely held

that claims directed to gathering and processing data are directed to an abstract idea."); *SAP*, 898 F.3d at 1167 ("The focus of the claims . . . is on selecting certain information, analyzing it using mathematical techniques, and reporting or displaying the results of the analysis. That is all abstract."); *Glasswall Solutions Ltd. v. Clearswift Ltd.*, 754 F. App'x 996, 998 (Fed. Cir. 2018) ("The claims merely require the conventional manipulation of information by a computer. We have often held similar conventional data manipulation to be abstract."); *Intellectual Ventures I LLC v. Capital One Fin. Corp.*, 850 F.3d 1332, 1340 (Fed. Cir. 2017) ("We have held other patent claims ineligible under § 101 for reciting similar data manipulation steps."); *Affinity Labs of Texas, LLC v. DIRECTV, LLC*, 838 F.3d 1253, 1261 (Fed. Cir. 2016) ("the conveyance and manipulation of information using wireless communication and computer technology" is an abstract idea); *Elec. Power*, 830 F.3d at 1353 ("Information as such is an intangible" so manipulating data, "including when limited to particular content (which does not change its character as information), [i]s within the realm of abstract ideas."); *Gottschalk v. Benson*, 409 U.S. 63, 65-73 (1972) (method of "converting signals" using mathematical operations is not patent eligible).

The claims' use of basic electronic hardware to carry out their function cannot bar a finding that the claims go to abstract ideas. *See, e.g.*, Ex. 1, '381 at claim 1 (well-known components include "field programmable gate array," "deserializer," "phase lock loop," and "computational circuitry"). For example, in *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1348 (Fed. Cir. 2019), the Federal Circuit held that a patent claiming a device and method for communicating a garage door's status (i.e., whether it was open or shut) was directed to an abstract idea, even though the claims had a physical component. *See id.* The "mere physical nature of" a claim's elements are "not enough to save the claims from abstractness" where such claims "us[e] off-the-shelf technology for its intended purpose." *See id*.

Indeed, in *Alice* itself, the Supreme Court held that "the fact that a computer necessarily exists in the physical, rather than purely conceptual, realm, is beside the point." *Alice*, 573 U.S. at 224 (cleaned up). That the method claims in the Asserted Patents require the use of physical hardware does not change that they are ultimately directed to the abstract idea of data manipulation. *See Am. Axle & Mfg., Inc. v. Neapco Holdings LLC*, 967 F.3d 1285, 1293 & n.3 (Fed. Cir. 2020) (method of manufacturing car parts directed to an abstract idea). The fact that the '305 patent requires a physical device likewise does not change the analysis—the claims are directed to the abstract idea of data manipulation regardless of whether a physical device is used in effecting the manipulation. *See ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 770 (Fed. Cir. 2019) (claim is not patent eligible even though "the abstract idea is associated with a physical machine that is quite tangible—an electric vehicle charging station").

Redwood Techs., LLC v. Netgear, Inc., 738 F. Supp. 3d 511, 524-25 (D. Del. 2024) is illustrative. There, the disputed patents claimed a variety of improvements to wireless communications systems, including a particular circuit. *See id.* at 525 (describing "modulator circuit . . . configured to send a signal" based on incoming data). The court found that the claim of the circuit was directed towards an abstract idea because the concepts underlying the device were "well-known in the art," and therefore "fail[ed] to recite an improvement in computer-related technology." So too, here, the physical device claimed in the '305 patent does not undermine the conclusion that the claim is of an abstract idea. *See also WiTricity Corp. v. Momentum Dynamics Corp.*, 563 F. Supp. 3d 309, 316 (D. Del. 2021) (claims to apparatus including an "optimizing circuit" were abstract).

The results-focused functional language employed by the claims of the Asserted Patents confirms the claims' abstract nature. The claims require the functional results of "receiving,"

"generating," "converting," "transmitting," and "performing . . . operations," but do "not sufficiently describe how to achieve these results in a non-abstract way." *Two-Way Media Ltd. v. Comcast Cable Commc'ns, LLC*, 874 F.3d 1329, 1337 (Fed. Cir. 2017); *Affinity Labs of Tex., LLC v. DIRECTV, LLC*, 838 F.3d 1253, 1258-59 (Fed. Cir. 2016) (claims abstract where they involved "the function of wirelessly communicating regional broadcast content to an out-of-region recipient," without specifying "a particular way of performing that function"). For example, the claims of each of the Asserted Patents require "performing . . . a set of operations" on data using "computational circuitry." Ex. 1, '381 patent at 28:42-45; Ex. 2, '286 patent at 29:3-6; Ex. 3, '305 patent at 28:46-54. But the claims do not specify how that step is achieved, including what type of "operations" are involved, how they are performed, or what the "computational circuitry" entails.

Nor do the claims use any "inventive technology for performing those functions." *Elec. Power*, 830 F.3d at 1354. There is nothing in the claim language or specification that indicates that the claimed components have any new capabilities beyond performing the generic functional steps of receiving, generating, converting, and transmitting data in a known and conventional manner. And any alleged benefit from practicing the claims flows from implementing the abstract idea using conventional devices as tools, not from any improvement to the capability of the components (e.g., a field programmable gate array and a phase lock loop) themselves. The claims simply utilize off-the-shelf, already-known components. *See BSG Tech LLC v. BuySeasons, Inc.*, 899 F.3d 1281, 1288 (Fed. Cir. 2018) ("These benefits, however, are not improvements to database functionality. Instead, they are benefits that flow from performing an abstract idea in conjunction with a well-known database structure."); *see also* § I.B below.

At best, the Asserted Patents suggest that having a "clock domain crossing circuit . . . creates a technical problem" to be solved, because such circuits can create delays in data

processing. Ex. 1 at 10:34-34; *see also id.* at 1:46-52 ("The prior art sought to address this problem by including a clock domain crossing circuit in the FPGA, however, these circuits inherently add a delay to the processing that takes place in the FPGA, which is not desirable since high frequency trading may include time-stamps that are accurate to the microsecond such that even small delays may present a large problem."). The claims themselves acknowledge, however, that the Asserted Patents do not solve any technical problem relating to the use of clock domain crossing circuits; instead, the claims avoid the use of clock domain crossing circuits altogether. Ex. 1, '381 patent at 28:49-51 ("said method does not use clock domain crossing operations that delay processing of the first set of parallel data streams"); *see also* Ex. 2, '286 patent at 29:40-43 ("wherein the first set of operations does not include clock domain crossing operations that delay processing of the first set of parallel data streams"); Ex. 3, '305 patent at 28:53-54 ("without use of a clock domain crossing circuit").

Simply repackaging the problem to be solved (clock domain crossing creates delays) as the solution to the problem (do not use clock domain operations that create delays) does nothing to advance the claims beyond the realm of abstract ideas. *See Am. Axle*, 967 F.3d at 1295 ("The Supreme Court has long held that claims that state a goal without a solution are patent ineligible."); *ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 769 (Fed. Cir. 2019) ("the specification cannot be used to import details from the specification if those details are not claimed"); *SAP*, 898 F.3d at 1167 (claims lack "specificity required to transform a claim from one claiming only a result to one claiming a way of achieving it"); *WiTricity*, 563 F. Supp. 3d at 320. This is especially true where the patents' alternative to clock domain crossing circuits, *i.e.*, phase lock loops, are well-known, as discussed below in the next section.

In sum, the focus of the claims is basic data manipulation using conventional, off-the-shelf components. That is an abstract idea, fundamentally ineligible for patent protection.

B. *Alice* Step 2: The Claims Are Implemented Using Generic Computer Components in a Conventional Way

At step two, the Court "consider[s] the elements of each claim both individually and as an ordered combination to determine whether the additional elements transform the nature of the claim into a patent-eligible application." *Id.* (internal quotation marks omitted). "These transformative elements must supply an 'inventive concept' that ensures the patent amounts to 'significantly more than a patent upon the [ineligible concept] itself.'" *BSG Tech LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1289-90 (Fed. Cir. 2018). Thus, claims must include "'additional features' [that] must be more than 'well-understood, routine, conventional activity.'" *Ultramercial, Inc. v. Hulu, LLC*, 772 F.3d 709, 715 (Fed. Cir. 2014) (11-step method of sending information invalid). "The appropriate question is *not* whether the entire claim as a whole was 'well-understood, routine [and] conventional'" but instead whether, "apart from" the abstract idea, the additional elements add anything inventive. *Chamberlain Grp., Inc. v. Techtronic Indus. Co.*, 935 F.3d 1341, 1348-49 (Fed. Cir. 2019) (emphasis added).

The claims of the Asserted Patents lack any inventive concept. As an initial matter, the abstract idea itself cannot supply the inventive concept. *See, e.g.*, *ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759, 774 (Fed. Cir. 2019) ("a claimed invention's use of the ineligible concept to which it is directed cannot supply the inventive concept"); *SAP*, 898 F.3d at 1168 ("What is needed is an inventive concept in the non-abstract application realm.").

The claims add nothing to the abstract idea of data processing except generic and conventional components—a field programmable gate array and a phase lock loop, a phase control circuit, or a phase detector. These components were well-known and in widespread use well before

the Asserted Patents. The background of the Asserted Patents acknowledges that it was known that "FPGAs[] may be used in applications that require fast processing since FPGAs allow for all computations to occur on a single chip that has massive fine-grained parallelism." Ex. 2 at 1:31-34. Indeed, the Asserted Patents concede that, at the time of the invention, FPGAs were already being "used in the financial industry in high frequency trading." *Id.* at 1:35-35, and disclose that numerous FPGAs were commercially available, including "XCVU3P-2FFVC1517E, Intel 1SG280LH3F55E3VG, Xilinx XCVU9P-2FLGA2104E the Vitrex® Ultrascale, the Vitrex® Ultrascale Plus, the Stratix® V, the Stratix® 10, XILINX XC3042, the Intel EP4CE6E22C8LN and the Lattice ICE40LP384-SG32, to name a few." *Id.* at 9:23-28. The Asserted Patents do not purport to improve the functionality of FPGAs themselves but instead carry out abstract ideas using generic, off-the-shelf FPGAs. *See SAP Am., Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1169-70 (Fed. Cir. 2018) ("these limitations require no improved computer resources InvestPic claims to have invented, just already available computers, with their already available basic functions, to use as tools in executing the claimed process"). The complaint reinforces that the claims call for nothing other than conventional, pre-existing FPGAs—the accused products use a Vitrex® UltraScale+ FPGA, an FPGA also listed in the Asserted Patents as being "currently available." *Compare* Dkt. 1-4 at 2 to Ex. 2 at 9:26.

The phase lock loop, phase control circuit, and phase detector used in the claims are similarly conventional, off-the-shelf components being used in a typical manner. Although the Asserted Patents use different names to identify these three components, HFT points to the same widely available computer chip as satisfying those limitations; namely, the Si5346. *See* Dkt. 1-4 at 11-13 (identifying Si5346 as "phase detector"); Dkt. 1-5 at 15-16 (identifying Si5346 as "phase control circuit"); Dkt. 1-6 at 13 (identifying Si5346 as "phase lock loop"). Based on the data sheet

HFT cites in the complaint, Si5346 was available in 2015, well before the Asserted Patents were filed in 2020, 2021, and 2022. *See* https://docs.rs-online.com/9a98/0900766b81411ff1.pdf at 1 (cited in Dkt. 1-4 at 11-13, Dkt. 1-6 at 12-13). Likewise, the Asserted Patents disclose that the commercially available "SI571 VXCO" can be used, Ex. 2 at 21:56-59, and that other phase lock loops were known, *id.* at 2 (prior-art references include "Phase Frequency Detector in PLL," "Phaselock Techniques," "Digital signal processing for an adaptive phase-locked loop controller," and "Time to Digital Converter used in All Digital PLL"). The Asserted Patents do not purport to have invented an improved phase lock loop but instead utilize these already-known components to implement abstract ideas. *See SAP*, 898 F.3d at 1169-70.

Likewise, the other components named in the claims are conventional, basic building blocks of field programmable gate arrays and circuits—components such as data pins, clock pins, output pins, deserializers, serializers, adjustable oscillators, and computational circuitry. *See, e.g.*, Ex. 2 at 13:18-31 (listing commercially available adjustable oscillators). And the Asserted Patents do not contend that they are improvements to these generic building blocks. *See Elec. Power*, 830 F.3d at 1355 ("The claims at issue do not require any nonconventional computer . . . components.").

Nor does "limiting the claims to the particular technological environment of" high frequency trading "transform them into patent-eligible applications of the abstract idea at their core." *Elec. Power*, 830 F.3d at 1354; *see also SAP*, 898 F.3d at 1169 ("[L]imitation of the claims to a particular field of information—here, investment information—does not move the claims out of the realm of abstract ideas."). Thus, the claims' invocation of "market data" does not supply an inventive concept. *E.g.*, Ex. 2, '286 patent at claim 1 ("a first serial data stream comprising market

data"; "a second serial data stream comprising order entry data"), claim 20 ("second serial data stream includes trading data"); Ex. 1, '381 patent at claims 2-3; Ex. 3, '305 patent at claims 20-22.

There is also nothing about the order combination of the claims' elements that supplies an inventive concept. Even considered together, each of the conventional components are used in precisely the conventional way they are meant to be used. The complaint makes that clear. The complaint alleges that the claimed phase lock loop is the Si5347, which, according to a data sheet provided by HFT, is a circuit that "integrates" phase lock loops to ensure output clocks are synchronized in frequency and phase with input clocks. Dkt. 1-4 at 15-16. In other words, the Si5347 is being put to use in exactly the way it was designed and intended to be used, and, according to HFT, in the same way as the claimed phase lock loop operates in the claims. Accordingly, synchronizing clock signals using a phase lock loop (like the Si5347) "was conventional at the time the patent was filed and could be performed with off-the-shelf technology." *Chamberlain*, 935 F.3d at 1349. Any latency benefits achieved from using a phase lock loop simply "flow from performing an abstract idea in conjunction with [] well-known" components designed and intended to work together. *BSG Tech LLC v. Buyseasons, Inc.*, 899 F.3d 1281, 1288 (Fed. Cir. 2018) (abstract idea of using comparison data in a database not patent eligible).

C. The Other Claims of the Asserted Patents Are Also Patent Ineligible

Claim 1 of the '381 patent and claim 1 of the '286 patent are representative of the patents as a whole, as the claims closely resemble each other and are based on the same abstract idea. *See Mobile Acuity Ltd. v. Blippar Ltd.*, 110 F.4th 1280, 1290 (Fed. Cir. 2024) ("Limiting the analysis of a § 101 challenge to representative claims is proper when the claims at issue are 'substantially similar and linked to the same' ineligible concept."). In addition, the complaint discusses only

claim 1 of the asserted patents. *See* Dkt. 1 at ¶¶ 23 (Count 1), 23 (Count 3); Dkt. 1-4 (claim 1 only); Dkt. 1-6 (claim 1 only).

Even if considered, the dependent claims of the Asserted Patents do not add limitations that make these claims patent eligible. For example, certain dependent claims specify the number of data streams used in the methods, which only reinforces that these claims are directed to the abstract idea of data manipulation. *See* Ex. 1, '381 patent at claims 9-10; Ex. 2, '286 patent at claims 11-15; Ex. 3, '305 patent at claims 9-15. Similarly, other dependent claims describe the order of certain data-manipulation operations. *See* Ex. 1, '381 patent at claims 4-7; Ex. 2, '286 patent at claims 16-18. None of these dependent claims either shift the focus from an abstract idea or add an inventive concept.

CONCLUSION

Citadel requests that the Court determine that the claims of the Asserted Patents are not patent eligible and dismiss the complaint with prejudice.

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Respectfully submitted,

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